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09/265,373	03/10/1999	HIROYUKI FUJITA	29284/481	4442

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KENYON & KENYON
1500 K STREET, N.W., SUITE 700
WASHINGTON, DC 20005

EXAMINER
NGUYEN, PHUONGCHAU BA

ART UNIT	PAPER NUMBER
2665	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

P12

Office Action Summary	Application No. 09/265,373	Applicant(s) FUJITA ET AL.	
	Examiner Phuongchau Ba Nguyen	Art Unit 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2-26-03 amendment* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Ball (5,583,855).

Regarding claim 1:

Ball discloses in figures 5-7 A multiplex conversion unit (fig.6) comprising four types of circuit packs including a high-speed interface circuit pack, a low-speed interface circuit pack, an add/drop multiplex circuit pack and a connecting circuit pack, wherein:

said low-speed interface circuit pack (5a-5h) accommodates one or a plurality of low-speed transmission lines (STM-1 or 2Mbps) and includes an output section (VC-4 TSA 3b, 3d, 3f) for outputting a low-speed signal containing one or a plurality of time slots received from said low-speed transmission line to a plurality of high-speed interface circuit packs, and a path switch section (TSI 10a-10d) for selecting one of the low-speed signals input from said high-speed interface circuit packs for each time slot as a low-speed signal to be transmitted to one or a plurality of said low-speed transmission lines accommodated;

said high-speed interface circuit pack (2a & 3a) accommodates at least a high-speed transmission line (STM-4) and is adapted to output/input a plurality of line signals each containing a predetermined number of time slots transmitted to and received from said high-speed transmission line accommodated, a plurality of line signals input/output by other high-speed interface circuit packs, and a plurality of low-speed signals input/output by said low-speed interface circuit packs, said high-speed interface circuit pack including a time slot assignment section (VC-4 TSA 3a) having a first time slot assignment function (VC-4 TSA 3a via #3 or #4) between a plurality of line signals received from the said high-speed transmission line accommodated and output to other high-speed interface circuit packs (VC-4 TSA 3b via #3) on the one hand and the output low-speed signal (VC-4 TSA 3b via #1; col.7, lines 23-27) on the other hand, and a second time slot assignment function (VC-4 TSA 3a via #1) between a plurality of line signals input (2a) from other high-speed interface circuit packs and transmitted to the high-speed transmission line (accommodated on the one hand and the input low-speed signal (VC-4 TSA 3b via #2; col.7, lines 23-27)on the other hand;

said add/drop multiplex circuit pack (TSI 10) is adapted to out/input a plurality of line signals input/output by each of said high-speed interface circuit packs (at P1) and a low speed signal containing one or a plurality of time slots input/output by each of the low-speed interface circuit packs (at P2, P3), said add/drop multiplex circuit pack including a time slot section (inherent at the TSI 10) having the time slot interchange function between a plurality of line signals and a plurality of low-speed signals, and a line switch section (inherent at the TSI 10) having a first line switch function for switching the line signal to be processed by said time slot interchange section and a second line switch function for switching the time slots of the line signal to be processed by said time slot interchange section using the time slot interchange function of said time slot interchange section {col.7, lines 23-27};

said connecting circuit pack (i.e., VC-4 #2 at node 1; col.8, lines 49-51) is adapted to input/output the low-speed signal input/output by the high-speed interface circuit pack as a low-speed signal input/output by another high-speed interface circuit pack; and

a plurality of high-speed interface circuit packs and a plurality of low-speed interface circuit packs are connected to each other through said connecting circuit pack in such a manner that the low-speed signals input/output by the high-speed interface circuit packs are input/output as low-speed signals input/output by another high-speed interface circuit pack.

Regarding claim 2:

Ball discloses in figures 5-7 a multiplex conversion unit comprising four types of circuit packs including a high-speed interface circuit pack, a low-speed interface circuit pack, an add/drop multiplex circuit pack and a connecting circuit pack, wherein:

said low-speed interface circuit pack (5a-5h) accommodates one or a plurality of low-speed transmission lines and includes an output section for outputting a low-speed signal containing one or a plurality of time slots received from said low-speed transmission line to a plurality of high-speed interface circuit packs, and a path switch section for selecting one of the low-speed signals input from said high-speed interface circuit packs for each

time low-speed interface circuit packs for each time slot as a low-speed signal to be transmitted to one or a plurality of said low-speed transmission lines accommodated;

said high-speed interface circuit pack (2a & 3a) accommodates at least a high-speed transmission line and is adapted to output/input a plurality of line signals each containing a predetermined number of time slots transmitted to and received from said high-speed transmission line accommodated, a plurality of line signals input/output by other high-speed interface circuit packs, and a plurality of low-speed signals input/output by said low-speed interface circuit packs, said high-speed interface circuit pack including a time slot assignment section (i.e., TSA 3a) having a first time slot assignment function between a plurality of line signals received from the said high-speed interface circuit packs on the one hand and the output low-speed signal on the other hand, and a second time slot assignment function between a plurality of line signals input from other high-speed interface circuit packs and transmitted to the high-speed transmission line accommodated on the one hand and the input low-speed signal on the other hand;

said add/drop multiplex circuit pack (TSI) is adapted to output/input a plurality of line signals input/output by each of said high-speed interface circuit packs and a low-speed signal containing one or a plurality of time slots input/output by each of the low-speed interface circuit packs, said add/drop multiplex circuit pack including a time slot section having the time slot interchange function between a plurality of line signals and a plurality of low-speed signals, and a line switch section (inherent at TSI) having a first line switch function for switching the line signal to be processed by said time slot interchange section and a second line switch function (inherent at TSI) for switching the time slots of the line signal to be processed by said time slot interchange section using the time slot interchange function of said time slot interchange section {col.7, lines 23-27};

said connecting circuit pack (i.e., VC-4 #2 at node 1; col.8, lines 49-51) is adapted to input/output the low-speed signal input/output by the high-speed interface circuit pack as a low-speed signal input/output by another high-speed interface circuit pack; and

the time slot assignment section (i.e., TSA 3a) of said high-speed interface circuit packs has the add/drop multiplex function of converting the line signals transmitted to and received from the high-speed transmission line into a plurality of low-speed signals directly output/input, the connecting circuit pack (i.e., VC-4 #1 or #2)in the first mode is replaced by an add/drop multiplex circuit pack, and the high-speed interface pack and the low-speed interface circuit pack are connected to the add/drop multiplex circuit pack in such a manner that a plurality of low-speed signals input/output by a plurality of high-speed interface circuit packs are output/input by said add/drop multiplex circuit pack as line signals output/input by a plurality of high-speed interface circuit packs, and the low-speed signals input/output by the add/drop multiplex circuit pack are output/input by the low-speed interface circuit pack as output/input low-speed signals.

Regarding Claims 3-4:

Ball further discloses that the multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring-UPSR (figs.8, 10-11) and Terminal

Multiplex-TM networks by selectively combining said four types of circuit packs.

3. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Furuta (5,600,648).

Regarding claims 1-2:

Furuta discloses in figure 19 a multiplex conversion unit comprising a high-speed interface circuit pack (30a), a low-speed interface circuit pack (30d), an add/drop multiplex circuit pack (20) and a connecting circuit pack (30b, 30c).

Regarding Claims 3-4:

Furuta further discloses that the multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring-UPSR (fig. 19) and Terminal Multiplex-TM networks by selectively combining said four types of circuit packs.

4. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Hurlocker (5,490,142).

Regarding claims 1-2:

Hurlocker discloses in figure 3 a multiplex conversion unit (110) comprising a high-speed interface circuit pack (112, 115), a low-speed interface circuit pack (145), an add/drop multiplex circuit pack (130, 170) and a connecting circuit pack (127).

Regarding Claims 3-4:

Hurlocker further discloses that the multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring-UPSR (fig.3) and Terminal Multiplex-TM networks by selectively combining said four types of circuit packs.

5. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto (5,546,403).

Regarding claims 1-2:

Yamamoto discloses in figures 4 &7 a multiplex conversion unit comprising a high-speed interface circuit pack (22, 21 at 2.4 Gbps), a low-speed interface circuit pack (DS3x48 at 45 Mbps), an add/drop multiplex circuit pack (Add, TSA, TSI, SEL) and a connecting circuit pack (Mux, Demux).

Regarding Claims 3-4:

Yamamoto further discloses that the multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring-UPSR (figs.2-7) and Terminal Multiplex-TM networks by selectively combining said four types of circuit packs.

6. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Shioda (5,537,393).

Regarding claims 1-2:

Shioda discloses in figures 5&7 a multiplex conversion unit comprising a high-speed interface circuit pack (13 at high order), a low-speed interface

circuit pack (add channel at low order), an add/drop multiplex circuit pack (20) and a connecting circuit pack (35, 21) {also, figs.3, 6, 8}.

Regarding Claims 3-4:

Shioda further discloses that the multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring-UPSR (figs.1-3, 5, 7-8) and Terminal Multiplex-TM networks by selectively combining said four types of circuit packs.

7. Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (5,799,001).

Regarding claims 1-2:

Lee discloses in figure 1 a multiplex conversion unit comprising a high-speed interface circuit pack (STM-N Signal), a low-speed interface circuit pack (DSn Signal), an add/drop multiplex circuit pack (Add-Drop Part) and a connecting circuit pack (HVC Connection Matrix){also, fig.2-4,10}.

Regarding Claims 3-4:

Lee further discloses that the multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring-UPSR (figs.3d-3e, 3g-3h, 3j-3k, 3m) and Terminal Multiplex-TM networks (figs.6-9) by selectively combining said four types of circuit packs.

8. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Hiramoto (5,471,476).

Regarding claims 1-2:

Hiramoto discloses in figures 4 and 7 a multiplex conversion unit comprising a high-speed interface circuit pack (oc-3 W), a low-speed interface circuit pack (Tel1, Trm2), an add/drop multiplex circuit pack (102 in fig.4; also see fig.7) and a connecting circuit pack (103).

Regarding Claims 3-4:

Hiramoto further discloses that the multiplex conversion unit is applicable to one of Uni-directional Path Switched Ring-UPSR (figs.4, 7) and

Terminal Multiplex-TM networks by selectively combining said four types of circuit packs.

9. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Takatsu (5,311,501).

Takatsu discloses in figure 1 a multiplex conversion unit comprising a high-speed interface circuit pack (70), a low-speed interface circuit pack (81-89), an add/drop multiplex circuit pack (72-75) and a connecting circuit pack (76-80).

Response to Arguments

10. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Lee, Hiramoto, Shioda, Yamamoto do not teach "if TSI function is not required, the circuit pack having the TSI function is replaced by the low cost connecting circuit pack to reduce the manufacturing cost of the entire node"; and Ball does not teach "allowing function addition by exchanging

a circuit pack having TSI function and detaching TSI circuit pack to reduce the cost of a node in a case that TSI function is unnecessary"; Furuta does not teach "a circuit pact together with interfaces, the line selection being realized by a low cost connecting circuit pack, and in case of the TSI function, the connecting circuit pack being replaced by the add/drop circuit pack"; Hurlocker does not teach "the cross connect function is unnecessary in case where the TSI alone is needed for reducing cost of nodes") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

11. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuongchau Ba Nguyen whose telephone number is 703-305-0093. The examiner can normally be reached on Monday-Friday from 10:00 a.m. to 3:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 703-308-6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

PN

Phuongchau Ba Nguyen
Examiner
Art Unit 2665

April 29, 2003

4/24/07